1. A programmable current booster circuit for an integrated circuit device comprising:

a first rising edge control circuit;

a first falling edge control circuit, wherein inputs of the first rising and first falling edge control circuits are coupled to a common input signal, and wherein the first rising edge and first falling edge control circuits are controlled based on input/output configuration signals from the integrated circuit device;

a first rising edge output current regulation circuit coupled to the output of the first rising edge control circuit; and

a first falling edge output current regulation circuit coupled to the output of the first falling edge control circuit, wherein outputs of the first rising edge current regulation circuit and the first falling edge current regulation circuit are coupled to provide a unified output signal.

2. The programmable current booster of Claim 1 further comprising:

at least a second rising edge control circuit;

at least a second falling edge control circuit, wherein the inputs of the at least a second rising and at least a second falling edge control circuits are coupled to the common input signal, and the at least a second rising edge and the at least a second falling edge control circuits are configurable based on input/ output configuration signals received from the integrated circuit device;

at least a second rising edge output current regulation circuit coupled to the output of the at least a second rising edge control circuit; and

at least a second falling edge output current regulation circuit coupled to the output of the at least a second falling edge control circuit;

wherein the first rising edge and first falling edge output current regulation circuits are coupled in parallel with the at least a second rising edge and the at least a second falling edge output current regulation circuits respectively, and the output of the circuits coupled in parallel are coupled to the unified output signal.

3. The programmable current booster circuit of Claim 1 wherein the first rising edge control circuit comprises:

a first inverter gate coupled to receive an input/output configuration signal from the integrated circuit device;

a NOR gate coupled to receive a first NOR input from an input/output configuration signal from the integrated circuit device;

an OR gate coupled to receive a first OR input from the first inverter gate, a second OR input from the NOR gate and a third OR input from the common input signal; and

a first programmable delay element having an input from the common input signal, the output of the first programmable delay element being coupled to a second NOR input of the NOR gate.

4. The programmable current booster of Claim 1 wherein the first rising edge current regulation circuit comprises at least one PMOS transistor.

5. The programmable current booster circuit of Claim 1 wherein the first falling edge control circuit comprises:

a NAND gate coupled to receive as a first NAND input an input/output configuration signal from the integrated circuit device;

a second programmable delay element having an input from the common input signal and having an output coupled to a second NAND input of the NAND gate; and

an AND gate coupled to have a first AND input from the output of the NAND gate, a second AND input coupled to the input of the second programmable delay element, and a third AND input from an input/ output configuration signal received from the integrated circuit device.

6. The programmable current booster of Claim 1 wherein the first falling edge current regulation circuit comprises at least one NMOS transistor.

7. The programmable current booster of Claim 1 wherein the first rising edge output current regulation circuit comprises:

an output transistor coupled to receive the output of the first rising edge control circuit;

a voltage source;

wherein the source terminal of the output transistor is coupled to the voltage source and the drain of the output transistor is coupled to the first falling edge current regulation circuit.

8. The programmable current booster of Claim 1 wherein the first falling edge output current regulation circuit comprises:

an output transistor coupled to receive the output of the first falling edge control circuit;

wherein the drain of the output transistor is coupled to the first rising edge current regulation circuit and the source terminal of the output transistor is connected to ground.

9. The programmable current booster of Claim 1 for use with an output driver of an integrated circuit device wherein the unified output signal conforms to at least one of the HSTL or SSTL signaling standards.

10. A printed circuit board on which is mounted an integrated circuit device comprising a programmable current booster circuit as defined in Claim 1.

11. A programmable current booster circuit for use with a differential output driver of an integrated circuit device comprising:

a pair of AC stage rising edge control circuits coupled to receive a pair of differential input signals, wherein the pair of differential input signals differ from one another in voltage in order to represent

information in accordance with a differential interface standard;

a pair of AC stage rising edge output current regulation circuits coupled to respective outputs of the AC stage rising edge control circuits;

a pair of DC stage rising edge control circuits coupled to receive the pair of differential input signals;

a pair of AC stage falling edge control circuits coupled to receive the pair of differential input signals;

a pair of AC stage falling edge output current regulation circuits coupled to respective outputs of the pair of AC stage falling edge control circuits; and

a pair of DC stage falling edge control circuits coupled to receive the pair of differential input signals;

wherein the pairs of AC and DC stage rising edge and AC and DC falling edge control circuits are configurable based on input/ output configuration signals received from the integrated circuit device and the outputs of the respective pairs of AC rising and falling edge current regulation circuits and the DC stage rising and falling edge control circuits are coupled in parallel to provide a pair of differential output signals.

12. The programmable current booster circuit of Claim 11 wherein the AC stage rising edge control circuit further comprises:

a first inverter gate coupled to receive an input/output configuration signal from the integrated circuit device;

a NOR gate coupled to receive a first NOR input from an input/output configuration signal from the integrated circuit device;

an OR gate coupled to receive a first OR input from the first inverter gate, a second OR input from the NOR gate and a third OR input from the common input signal received from the integrated circuit device; and

a first programmable delay element having an input from the common input signal received from the integrated circuit device, the output of the first programmable delay element being coupled to a second NOR input of the NOR gate.

13. The programmable current booster circuit of Claim 11 wherein the DC stage rising edge control circuit further comprises:

an OR gate having a first OR input from the common input signal received from the integrated circuit device, a second OR input from an input/ output

configuration signal received from the integrated circuit device, and a third OR input coupled to the second OR input;

an output transistor coupled to receive the output of the OR gate, having its drain coupled to a respective one differential output signal, and its source terminal coupled to a voltage source via a current source.

14. The programmable current booster circuit of Claim 11 wherein the DC stage rising edge control circuit comprises at least one PMOS transistor.

15. The programmable current booster circuit of Claim 11 wherein the AC stage falling edge control circuit further comprises:

a NAND gate coupled to receive as a first NAND input an input/output configuration signal from the integrated circuit device;

a second programmable delay element having an input from the common input signal received from the integrated circuit device and having an output coupled to a second NAND input of the NAND gate; and

an AND gate coupled to have a first AND input from the output of the NAND gate, a second AND input coupled to the input of the second programmable delay element, and a third AND input from an input/ output

configuration signal received from the integrated circuit device.

16. The programmable current booster circuit of Claim 11 wherein the DC stage falling edge control circuit further comprises:

an AND gate coupled to receive a first AND input from the common input signal received from the integrated circuit device, a second AND input from an input/output configuration signal received from the integrated circuit device, and a third AND input coupled to the second AND input; and

an output transistor coupled to receive the output of the AND gate, having its drain coupled to a respective one differential output signal and its source terminal coupled to ground via a current source.

17. The programmable current booster circuit of Claim 11 wherein the DC stage falling edge control circuit comprises at least one NMOS transistor.

18. The programmable current booster of Claim 11 wherein each one AC stage rising edge output current regulation circuit includes at least one PMOS transistor.

19. The programmable current booster of Claim 11 wherein each one AC stage falling edge output current regulation circuit includes at least one NMOS transistor.

20. The programmable current booster of Claim 11 for use with a differential output driver of an integrated circuit device wherein the pair of differential output signals are further conditioned to conform to minimum and maximum limits for current and voltage as specified by a differential signaling standard.

21. A printed circuit board on which is mounted an integrated circuit device comprising a programmable current booster circuit for use with a differential output driver as defined in Claim 11.

22. The programmable current booster of Claim 11 for use with a differential output driver of an integrated circuit device wherein the pair of differential output signals conforms to at least one of the LVDS, HT or LVPECL signaling standards.